Notice of Allowability	Application No.	Applicant(s)	
	10/614,642.	DIXIT ET AL.	
	Examiner	Art Unit	
	Cynthia Britt	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *5/30/06*.

2. ☒ The allowed claim(s) is/are *1-2, 5-14, 17-24 and 26-30 (now renumbered1-25)*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☒ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☒ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date 2/24/06.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Drawings

The proposed drawing changes submitted 5/30/06 are acceptable. Replacement sheets are required.

REASONS FOR ALLOWANCE

The following is an examiner's statement of reasons for allowance:

The present invention pertains to a system and method for testing data retention of a memory. The present invention claims (claim 1 as representative) features such as "...pausing for a predetermined time interval during a third time period subsequent to said second time period if the total time required to write said first data to said first memory sub-group and said second data to said second memory sub-group is insufficient to determine data retention capabilities of said first and second memory sub-groups;...".

The prior arts of record (Nakamura et al. U.S. Patent No. 7,064,998 as an example of such prior arts) teach " The first memory unit writes first write data to the memory cell in response to the first write signal. The second memory unit writes second write data to the memory cell in response to the second write signal. The first and second memory units operate independent of each other in accordance with the first and second write signals, respectively. Consequently, no matter what timing the write enable signal and the first and second data enable signals are supplied at, the write control circuit has only to output the first and second write signals at predetermined timing in accordance with these control signals. In other words, the write control circuit

need not make a control such as shifting of the start timing of a write operation in accordance with the supply timing of the control signals. This allows a reduction in the circuit scale of the semiconductor memory and improves the timing margin of the write control circuit. As a result, it is possible to reduce the write cycle time." And, "A memory core has a memory cell that requires a refresh for the sake of data retention. A refresh control circuit generates a refresh command to refresh the memory cell at predetermined intervals." The prior arts however, fail to teach "...pausing for a predetermined time interval during a third time period subsequent to said second time period if the total time required to write said first data to said first memory sub-group and said second data to said second memory sub-group is insufficient to determine data retention capabilities of said first and second memory sub-groups;...". As such, modification of the prior arts of record can only be motivated by hindsight reasoning, or by changing the intended use and function of the prior arts themselves. Therefore, it is not clear that one of ordinary skill in the art at the time of the invention would have made the necessary modifications to the prior arts of record to encompass the limitations set forth in the present application. Moreover, none of the prior arts of record, taken either alone or in combination, anticipate nor render obvious the claimed inventions. Hence, claims 1-2, 5-14, 17-24 and 26-30 are allowable over the prior arts of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

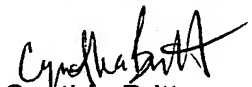
JP 11149798 A Watanabe

This patent teaches in order to reduce the number of test patterns of a semiconductor integrated circuit incorporating a plurality of memory cells with data input of the same number of bits and different capacity, and easily test the semiconductor integrated circuit, it is judged whether the address of the maximum capacity memory cell 20 corresponds to memory cells 17-19 or not using address detection circuits 11 and 12 and the most significant bit signal 13, and output data selection circuits 14, 15, and 16 select the output data of memory cells 17-19 and the maximum capacity memory cell 20 and output them. In write data retention circuits 24-26 and address control circuits 21-23, a flag value 0 is set to the output of the address detection circuits 11 and 12 and the most significant bit signal 13, an address signal is fixed, and write data are retained, thus suppressing malfunction and simultaneously testing the memory cells 17-19 by the same test pattern.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Cynthia Britt
Primary Examiner
Art Unit 2138

Atty Docket 4028-03200 (03-0169)

OK to Enter 6/6/06

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Charutosh Dixit, et al.	§	
		§	Group Art Unit: 2138
Serial No.:	10/614,642	§	
		§	Examiner: Britt, Cynthia H.
Filed:	July 7, 2003	§	
		§	Confirmation No.: 7652
For:	Method and System of Testing Data Retention of Memory	§	

Commissioner for Patents
Mail Stop Amendment
P.O. Box 1450
Alexandria, VA 22313-1450

Certificate of Mailing

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class mail in an envelope addressed to: Commissioner for Patents, Mail Stop Amendment, P.O. Box 1450, Alexandria, VA 22313-1450, on:

M. J. Z. May 24, 2006

Signature Date of Deposit

REQUEST FOR APPROVAL OF PROPOSED DRAWING CORRECTION

Attached hereto is one (1) sheet of proposed drawing corrections with the proposed changes marked in red. The foregoing changes are intended to provide descriptive labels for the elements of system 200 illustrated in Figure 2. More specifically, the Applicants propose that each element 210 be labeled a "memory sub-group", that element 230 be labeled a "test controller and that elements 240a and 240b each be labeled a "memory controller."

It is submitted that the proposed changes are fully supported by paragraphs 34-37 of the specification and do not, therefore, introduce new matter to the application. Accordingly, the Applicants respectfully request approval of this request. Upon approval of the proposed drawing correction and upon an indication of allowable subject matter, the Applicants shall submit Replacement Drawings incorporating all of the proposed drawing corrections approved by the Examiner.

No fees are believed to be required. If, however, any fees are deemed necessary, please charge these fees to LSI Logic Corporation, Deposit Account No. 12-2252. Further, no extension of time is believed to be necessary. If, however, an extension of time is believed to be required, please charge any fees for this extension to LSI Logic Corporation, Deposit Account No. 12-2252.

Respectfully submitted,

Date: MAY 24, 2006

Michael S. Bush
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ok to enter 7/6/06 CB

A Method And System of Testing Data Retention Of Memory
Atty Dkt: 03-0169 (4028-03200)
Inventors: Carutosh Dixit, et al

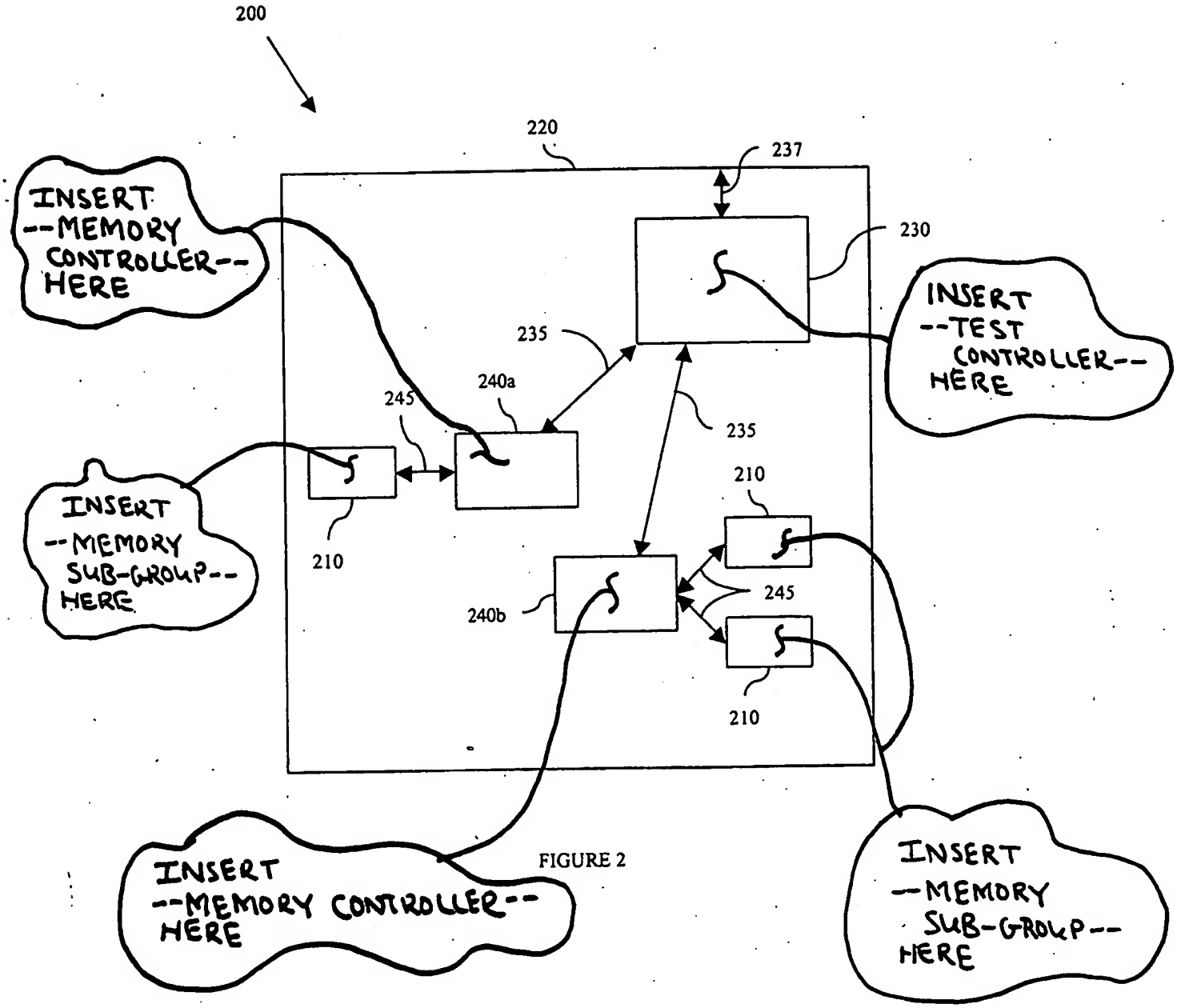

FIGURE 2